CLAIMS

What is claimed is:

1. An apparatus comprising:

a first drain bias network having an input suitable to couple to a FLASH cell;

a second drain bias network having an input suitable to couple to a FLASH cell; and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit.

2. The apparatus of claim 1 further comprising:

a sense amplifier having a first input, a second input, and an output; and wherein:

the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

3. The apparatus of claim 2 further comprising:

a reference FLASH cell coupled to the second drain bias network; and

a FLASH cell coupled to the first drain bias network.

4. The apparatus of claim 3 wherein:

the reference FLASH cell coupled to the second drain bias network through a reference column select transistor and the FLASH cell selectively coupled to the first drain bias network through a column select transistor, the column select transistor controlled by a column select signal.

5. The apparatus of claim 2 further comprising:

a FLASH cell coupled to the first drain bias network.

6. The apparatus of claim 5 wherein:

the FLASH cell selectively coupled to the first drain bias network through a first column select transistor.

7. The apparatus of claim 6 further comprising:

a reference FLASH cell coupled through a second column select transistor to the second drain bias network.

8. The apparatus of claim 7 wherein:

the equalization circuit is a transistor having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control electrode coupled to a third node of the transistor, the control electrode to deliver the control signal.

9. The apparatus of claim 4 wherein:

the equalization circuit is a transistor having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control electrode coupled to a third node of the transistor, the control electrode to deliver the control signal.

10. The apparatus of claim 2 further comprising:

a reference FLASH cell coupled to the second drain bias network.

11. The apparatus of claim 10 wherein:

the reference FLASH cell coupled to the second drain bias network through a reference column select transistor.

12. A method comprising:

equalizing a sense input and a reference input;

coupling the sense input to a FLASH cell to be sensed;

terminating equalization of the sense input and the reference input; and

measuring a sense voltage, the sense voltage corresponding to the sense input.

13. The method of claim 12 further comprising:

selecting the FLASH cell.

14. The method of claim 13 wherein:

coupling further includes loading the FLASH cell with a load.

15. The method of claim 14 further comprising:

coupling the reference input to a reference FLASH cell, including loading the reference FLASH cell;

measuring a reference voltage, the reference voltage corresponding to the reference input; and

comparing the sense voltage and the reference voltage.

16. An apparatus comprising:

a first bias means for biasing a FLASH cell, the first bias means having an input and an output;

a second bias means for biasing a reference FLASH cell, the second bias means having an input and an output; and

an equalization means for selectively equalizing the input of the first bias means and the input of the second bias means, the equalization means coupled to the input of the first bias means and coupled to the input of the second bias means.

17. The apparatus of claim 16 further comprising:

a comparison means for comparing the output of the first bias means and the output of the second bias means.

18. The apparatus of claim 17 further comprising:

a FLASH cell selectively coupled to the input of the first bias means; and

a reference FLASH cell coupled to the input of the second bias means.

19. The apparatus of claim 18 wherein:

the input of the first bias means is disposed at a first node of the first bias means and the output of the first bias means is also disposed at the first node of the first bias means; and

the input of the second bias means is disposed at a first node of the second bias means and the output of the second bias means is also disposed at the first node of the second bias means.

20. A FLASH device comprising:

a FLASH cell array;

a control circuit block coupled to the FLASH cell array to control the FLASH cell array; and

a comparison circuit block coupled to the FLASH cell array and coupled to the control circuit block, the control circuit block to control the comparison circuit, the comparison circuit including:

a first drain bias network having an input suitable to couple to a FLASH cell,

a second drain bias network having an input suitable to couple to a FLASH cell, and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit..

21. The FLASH device of claim 20, further comprising:

a sense amplifier having a first input, a second input, and an output; and wherein:

the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

22. The FLASH device of claim 21 further comprising:

a reference FLASH cell coupled through a column select transistor to the input of the second drain bias network; and wherein:

a selected FLASH cell of the FLASH cell array selectively coupled through a column select transistor to the input of the first drain bias network.

23. The FLASH device of claim 22 further comprising:

a power supply circuit coupled to the control circuit block and to the FLASH cell array and to the comparison circuit block.

24. An apparatus comprising:

a first bias network having an input suitable to couple to a persistent memory storage location;

a second bias network having an input suitable to couple to a persistent memory storage location; and

an equalization circuit having a first node coupled to the input of the first bias network and having a second node coupled to the input of the second bias network and having a control signal to control operation of the equalization circuit.

25. The apparatus of claim 24 further comprising:

a sense amplifier having a first input, a second input, and an output; and wherein:

the first bias network has an output coupled to the first input of the sense amplifier and the second bias network has an output coupled to the second input of the sense amplifier, the output of the first bias network having a relationship with the input of the first bias network, the output of the second bias network having a relationship with the input of the second bias network.

26. The apparatus of claim 25 further comprising:

a reference persistent memory storage location coupled to the second bias network through a reference column select circuit and a persistent memory storage location selectively coupled to the first bias network through a column select circuit, the column select circuit controlled by a column select signal.